

XpressVUP - LP9PI

2 x 100G Ethernet Processing FPGA Board For critical fanless applications

 Conduction cooled heat spreader equipped with a low-profile PCIe Virtex Ultrascale+ VU9P FPGA board

- Acrylic coating, Industrial temp grade
- PCle Gen3 x16 interface
- 2 banks of DDR4, 16GByte total
- 2 banks of QDR2+, 576 Mbit total
- Dual QSFP28 cages 10GbE/40GbE/100GbE







Target applications:

Industrial fanless systems

Defense ruggedized systems





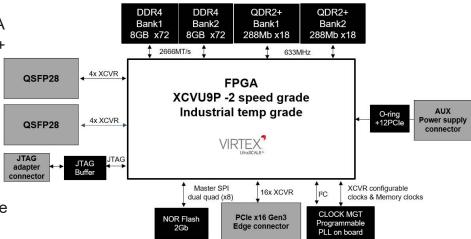




XpressVUP-LP9PI

Benefits

- AMD Virtex UltraScale+ VU9P FPGA
- On board two DDR4 and two QDR2+ independent banks
- Two QSFP28 optical cage for multi networking solutions
- PCIe endpoint with 16 lanes at 8 Gb/s link rate (Gen3)
- Fail safe configuration flash sector capability
- Tandem configuration mode available
- JTAG connector



Full Specifications

FPGA and Configuration Modules

- AMD Virtex UltraScale+ 16nm FPGA = XCVU9P-2FLGB2104I
- 2,6 M System Logic Cells, 270 Mb UltraRAM
- JTAG connector for external Xilinx USB cable
- 2x Nor Flash for dual quad SPI (x8) configuration mode

Communication Interfaces

- PCI Express x16 (Gen 1, 2 or 3)
- 2 x QSFP28 quad optical cage (2 x 4 XCVR : 28 Gb/s per link)
 - 10 GbE/25GbE/50GbE/100GbE/2 x 100GbE networking interface
 - Other protocols supported by the QSFP28 modules

Memory

- On board DDR4, 2x banks by 64 bit + 8 bitsECC, total 16GB
- On board QDR2+, 2x banks by 18 bit, total 576Mbit

Power

Max 120W

Other resources

On board programmable PLL oscillator (Si5345), highly flexible and configurable clock generator

Dissipation

- Operating range : -40°C to 70°C
- Industrial temp grade Bill of Material components
- Conduction cooled up to 70°C onto the heat spreader

Mechanical dimensions (board + heat spreader)

Length: 215.70mmHeight: 93.83mmThickness: 24.9mm

Standards and compliance

- Acrylic coating
- RoHS/REACH compliant
- UL certified
- ISO9001 Facility

Deliverables

- PCIe board equiped with conduction cooled heatsink
- PCIe AUX power cable adaptor
- JTAG adaptor cable to USB

- XpressVUP Board Support Package
 - Reference Manual
 - HDL designs, Vivado 2023.1
 - PCIe Reference Design using AMD Xilinx QDMA IP
- Mechanical files: 3D DWF/STEP models and 2D CAD drawing (upon request)

Ordering information

Part number

Description

- XpressVUP-LP9PI
- VU9P speed grade -2; 2 bank DDR4 by 72bit of 16GByte total @2666MT/s;
 2 banks QDR2+ by 18bit of 288Mbit each @550Mhz, Indus temp grade, conduction cooled heat spreader